

being digital values;

Figs. 5A, 5B, and 5C show AND/OR reconfigurable logic circuits with E/E, E/D, and CMOS inverter structures;

5 Fig. 6 illustrates an example structure of a NAND/NOR reconfigurable logic circuit, with a CMOS inverter for an input;

Fig. 7 illustrates an AND/OR circuit with a n-channel spin MOSFET of a depletion type;

10 Fig. 8 shows the operating curve of an AND/OR circuit with the n-channel spin MOSFET of a depletion type;

Fig. 9A and 9B are truth tables of the AND/OR circuit with the n-channel spin MOSFET of a depletion type;

15 Fig. 10 illustrates a circuit that has a XNOR function added to the circuit illustrated in Fig. 7;

Fig. 11 illustrates a first operation of the circuit illustrated in Fig. 10;

20 Fig. 12A shows the operating curve of the AND/OR function;

Fig. 12B shows a truth table of the OR circuit;

Fig. 12C shows a truth table of the AND circuit;

25 Fig. 13A shows the operating curve of the XNOR function;

Fig. 13B shows a truth table of the XNOR circuit;

Fig. 14A illustrates a third operation of the circuit illustrated in Fig. 10;

Fig. 14B is a truth table of the operation;

30 Fig. 15 illustrates the structure of a circuit that can reconfigure all the symmetric Boolean functions;

Fig. 16A illustrates the circuit structure of a threshold value variable inverter;

35 Fig. 16B illustrates an example operation of the inverter;

Fig. 17 has the threshold value of a conventional

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CMOS inverter as the function of the ratio of  $\beta$  of a pMOS to  $\beta$  of an nMOS;

Fig. 18 illustrates an example structure of an AND/OR circuit;

5 Fig. 19A shows a first operation of the circuit illustrated in Fig. 18;

Fig. 19B shows a truth table of the operation;

Fig. 20A shows a second operation of the circuit illustrated in Fig. 18;

10 Fig. 20B shows a truth table of the operation;

Fig. 21 shows another example structure of an AND/OR circuit;

Fig. 22A shows the characteristics of the variable threshold value inverter of Fig. 21;

15 Fig. 22B shows a truth table of the inverter;

Fig. 23A corresponds to Fig. 22A, showing the operation when the threshold value is varied;

Fig. 23B corresponds to Fig. 22B, showing truth table;

20 Fig. 24 illustrates an example structure of an AND/OR/XNOR circuit;

Fig. 25 shows the operating curve of  $V_{in\_n}$  of the circuit illustrated in Fig. 24;

25 Fig. 26A shows a first operation of the circuit illustrated in Fig. 24;

Fig. 26B shows a truth table of the operation;

Fig. 27A shows a second operation of the circuit illustrated in Fig. 24;

Fig. 27B shows a truth table of the operation;

30 Fig. 28A shows a third operation of the circuit illustrated in Fig. 24;

Fig. 28B shows a truth table of the operation;

Fig. 29A shows a fourth operation of the circuit illustrated in Fig. 24;

35 Fig. 29B shows a truth table of the operation;

Fig. 30 illustrates an example structure of an AND/OR/XOR/XNOR circuit;